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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,870	06/27/2003	Mark T. Bohr	42P15335	7488

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,870	BOHR ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7,8,10-16,28 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 7, 8, 10-16, 28, and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 06/07/2006.

Claims 1-4, 7, 8, 10-16, 28, and 29 are active in this application.

Claim(s) 5, 6, 9, and 17-27 have been cancelled.

Remarks

2. Applicant's argument(s), filed 08/10/2006 have been fully considered, but are not persuasive.

Particularly, Examiner do/does not agree with Applicant's argument(s) that Chau in view of Kwon does not teach or suggest "an etch stop layer conformally disposed on the substrate on the second device exclusive of the first device." Fig. 12 of Kwon, for example, clearly shows that etch stop layer(s) 332a & 334a conformally disposed only on the substrate 300 on the second device (which is formed in/on active region 20). Etch stop layer(s) 332a & 334a is/are formed on both sides of the second gate electrode 306b, yet etch stop layer(s) 332a & 334a is/are not formed on the first device (which is formed in/on active region 10).

Similarly, figs. 21 and 24 clearly show that layer(s) 432(a) &434(a) are conformally disposed only on the second device (20), but not on the first device (10).

For these reasons, it is believed that the previous rejection should be retained and rewritten below, in view of the newly amendment(s).

Claim Rejections - 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim(s) 1-4, 7, 8, 10-16, 28, and 29 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,165,826 to Chau et al., in view of Kwon, US Patent Application Publication No. 2003/0025163.

Regarding claim 1, Chau discloses an apparatus, as shown in figs. 3(A-H), for example, comprising:

a substrate 300;

a first device (PMOS 360) including a gate electrode 308 on a surface of the substrate 300 in an area of the substrate defined by a first well 304; and

a single crystal silicon alloy material 322 (col. 8, line 17 to col. 9, line 8) disposed in each of a first junction region and a second junction region in the substrate adjacent the gate electrode 308 of the first device 360, wherein (a) a lattice spacing of the silicon alloy material 322 is different than a lattice spacing of a material of the first well 304 of

the substrate (see col. 6, lines 1-27; col. 8, lines 41-45; col. 9, lines 9-20), and (b) a surface of the first junction region 322 and a surface of the second junction region 322 are in a non-planar relationship with the surface of the substrate 300 (fig. 3H); and

a second device (NMOS) complementary to the first device (PMOS) and comprising junction regions 334 defined by doped portions of a material of a second well 302 of the substrate 300, the material of the second well 302 having a conductivity type (p-type) different than a conductivity type of the first well (n-type) (col. 6, lines 1-27).

Chau is silent about an etch stop layer conformally disposed on the substrate on the second device exclusive of the first device.

Kwon discloses an apparatus, as shown in figs. 11, 12, 18-21, and 24, comprising an etch stop layer (layer(s) 332a &334a in figs. 12, 18-20, or layer(s) 432(a) & 434(a) in figs. 21&24) conformally disposed on the substrate on a second device (20) exclusive of a first device (10). See paras. [0046], [[0056], [0059].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Chau to further include the etch stop layer(s), as those of Kwon, to prevent the silicide layer from being overetched in a subsequent process for forming contact holes. See paragraph [0043] of Kwon.

Regarding claim 2, Chau/Kwon discloses the apparatus wherein a surface 301 (fig. 3A) of the substrate 300 defines a top surface of the substrate and the surface of the first junction region 322 and the surface of the second junction region 322 are superior to the top surface of the substrate. See figs. 3(A-H) of Chau.

Regarding claim 3, Chau/Kwon discloses the apparatus wherein the surface of the first junction region 322 and the surface of the second junction region 322 are superior to the top surface of the substrate by a length in the range of between 5 nanometers and 150 nanometers. See figs. 3(D-F), and col. 8, lines 31-35 of Chau.

Regarding claim 4, Chau/Kwon discloses the apparatus wherein the first junction region 322 and the second junction region 322 define a depth in the range of between 30 nanometers and 250 nanometers in depth below the surface of the substrate. See figs. 3(D-F), and col. 8, lines 31-35 of Chau.

Regarding claim 7, Chau/Kwon discloses the apparatus wherein the lattice spacing of the silicon alloy material 322 is larger than the lattice spacing of the material of the first well of the substrate 304. See col. 6, lines 1-27; col. 8, lines 41-45; col. 9, lines 9-20 of Chau.

Regarding claim 8, Chau/Kwon discloses the apparatus wherein a surface of the substrate proximate to the first junction region 322 defines a first substrate sidewall

surface (along trench 305) and a surface of the substrate proximate to the second junction region 322 defines a second substrate sidewall surface (along other trench 305) and the silicon alloy material 322 disposed in the first junction region is attached to the first substrate sidewall surface and the silicon alloy material 322 disposed in the second junction region is attached to the second substrate sidewall surface. See figs. 3(E-H) of Chau.

Regarding claim 10, Chau/Kwon discloses the apparatus wherein the silicon alloy material 322 comprises one of silicon germanium ($Si_{y-x}Ge_x$), silicon carbide ($Si_{y-x}C_x$), nickel silicide (NiSi), titanium silicide ($TiSi_2$), and cobalt silicide ($CoSi_2$). See col. 8, line 17 to col. 9, line 8 of Chau.

Regarding claim 11, Chau/Kwon discloses the apparatus further comprising a layer of silicide material 342 on the surface of the first junction region 322, the surface of the second junction region 322, and the gate electrode 306/308, wherein the layer of silicide material comprises one of nickel silicide (NiSi), titanium silicide ($TiSi_2$), and cobalt silicide ($CoSi_2$). See col. 11, line 66 to col. 12, line 26 of Chau.

Regarding claim 12, Chau/Kwon discloses the apparatus further comprising a layer of conformal etch stop material 326 on the layer of silicide material, wherein the layer of etch stop material comprises one of silicon dioxide (SiO_2), phosphosilicate glass

(PSG, a Phosphorous doped SiO_2), silicon nitride (Si_3N_4), and silicon carbide (SiC). See figs. 3, 5 of Chau.

Regarding claim 13, Chau/Kwon discloses the apparatus further comprising a layer of dielectric material 326/506 comprising on the layer of conformal etch stop material, wherein the layer of dielectric material comprises one of carbon doped oxide (CDO), cubic boron nitride (CBN), silicon dioxide (SiO_2), phosphosilicate glass (PSG), silicon nitride (Si_3N_4), fluorinated silicate glass (FSG), and silicon carbide (SiC). See figs. 3, 5 of Chau.

Regarding claim 14, Chau discloses an apparatus, as shown in figs. 3(A-H), for example, comprising:

a substrate 300;

a first device (PMOS 360) including a gate electrode 308 on a surface of the substrate 300 and a first junction region 336 and a second junction region 336 in the substrate 300 adjacent the gate electrode 308, the first junction region 336 and the second junction region 336 defining a channel in a first well 304 of the substrate 300; and

a single crystal silicon alloy material 322 (col. 8, line 17 to col. 9, line 8) disposed in each of the first junction region 336 and the second junction region 336 such that a surface of the first junction region and a surface of the second junction region are superior to the top surface of the surface of the substrate by a length sufficient to cause

a strain in the first well 304 of the substrate (fig. 3H), wherein a lattice spacing of the silicon alloy material is different than a lattice spacing of a material of the well of the substrate (see col. 6, lines 1-27; col. 8, lines 41-45; col. 9, lines 9-20); and

a second device (NMOS) complementary to the first device (PMOS) and comprising a gate electrode 306 on the surface of the substrate 300 and junction regions 334 defined by doped portions of a material of a second well 302 of the substrate 300, wherein the material of the second well 302 of a conductivity type (p-type) different than a conductivity type (n-type) of the first well (col. 6, lines 1-27).

Chau is silent about an etch stop layer conformally disposed on the substrate on the second device exclusive of the first device.

Kwon discloses an apparatus, as shown in figs. 11, 12, 18-21, and 24, comprising an etch stop layer (layer(s) 332&334 in figs. 12, 18-20, or layer(s) 432(a)&434(a) in figs. 21&24) conformally disposed on the substrate on a second device (20) exclusive of a first device (10). See paras. [0046], [[0056], [0059].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Chau to further include the etch stop layer(s), as those of Kwon, to prevent the silicide layer from being overetched in a subsequent process for forming contact holes. See paragraph [0043] of Kwon.

Regarding claim 15, Chau/Kwon discloses the apparatus wherein the first well 304 of the substrate 300 comprises an N-type material having an electrically negative charge, and wherein the silicon alloy material 322 comprises a P-type junction region material having an electrically positive charge. See col. 6, lines 1-27; and col. 8, lines 41-45 of Chau.

Regarding claim 16, Chau/Kwon discloses the apparatus wherein the silicon alloy 322 is silicon germanium having a lattice spacing that is larger than a lattice spacing of the N-type channel/well material, and wherein the strain is a compressive strain. See col. 6, lines 1-27; col. 8, lines 41-45; col. 9, lines 9-20 (silicon germanium alloy 322 and diffused semiconductor regions 336 are formed on top of well region 304; therefore, alloy 322 and/or regions 336 must definitely produce a compression, or a compressive strain, on the well region 304) of Chau.

Regarding claims 28 and 29, Chau/Kwon discloses the apparatus wherein the second device (NMOS) comprises a gate electrode 306 on the surface of the substrate 300, the apparatus further comprising:

relative to an area defined by the first well 304 and an area defined by the second well 302, and etch stop layer 326 selectively disposed on the surface of the substrate in an area defined by the second well 302 such that the gate electrode 306 of the second device is disposed between the etch stop layer 326. See figs. 3 of Chau.

Conclusion

5. **THIS ACTION IS MADE FINAL.** A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday 9:00am - 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571)272-1907. The fax numbers for all communication(s) is (571)273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

Dao H. Nguyen
Art Unit 2818
October 26, 2006